6.4 Far Front Ends (WBS 2.3.2)

6.4.1 General

The front end readout for the MINOS detector is based on the VA chip series from IDE Corp. (Oslo, Norway). This chip provides a charge sensitive preamplifier, a shaper, sample/hold for each channel and is followed by an analog output multiplexer. The VA chip series was originally designed and used for silicon detectors, but it has also found use in non-silicon applications such as cathode pad readout in the Cleo3 RICH detector. Hamamatsu is currently developing a PMT base using the VA chip as well.

Typically, IDE markets this device by tailoring features to customer needs. Features that are easily adjusted are gain (preamp feedback capacitor), shaping time, and number of channels. We will have the first two adjusted for our needs. The ideal match to an M16 PMT is a 16 channel device. Since a 32 channel VA chip is already quite small, there is no financial incentive to produce a 16 channel version and so we will use the VA32 with half of the chips' channels unused.

6.4.2 Locations of the electronics components

The physical layout of the electronics for the far detector is shown in Figure 6.8.

The front end units are arranged evenly along the length of the far detector, attached to the MUX boxes. Each side of each supermodule is served by a single row of 4 readout crates at an intermediate height. The readout crates are spaced about 3.5 m apart, with their front end units 5 to 6 m away. All readout crate-to-front-end cables are equal in length for equal clock propagation delay. Each readout crate serves up to 32 front end units.

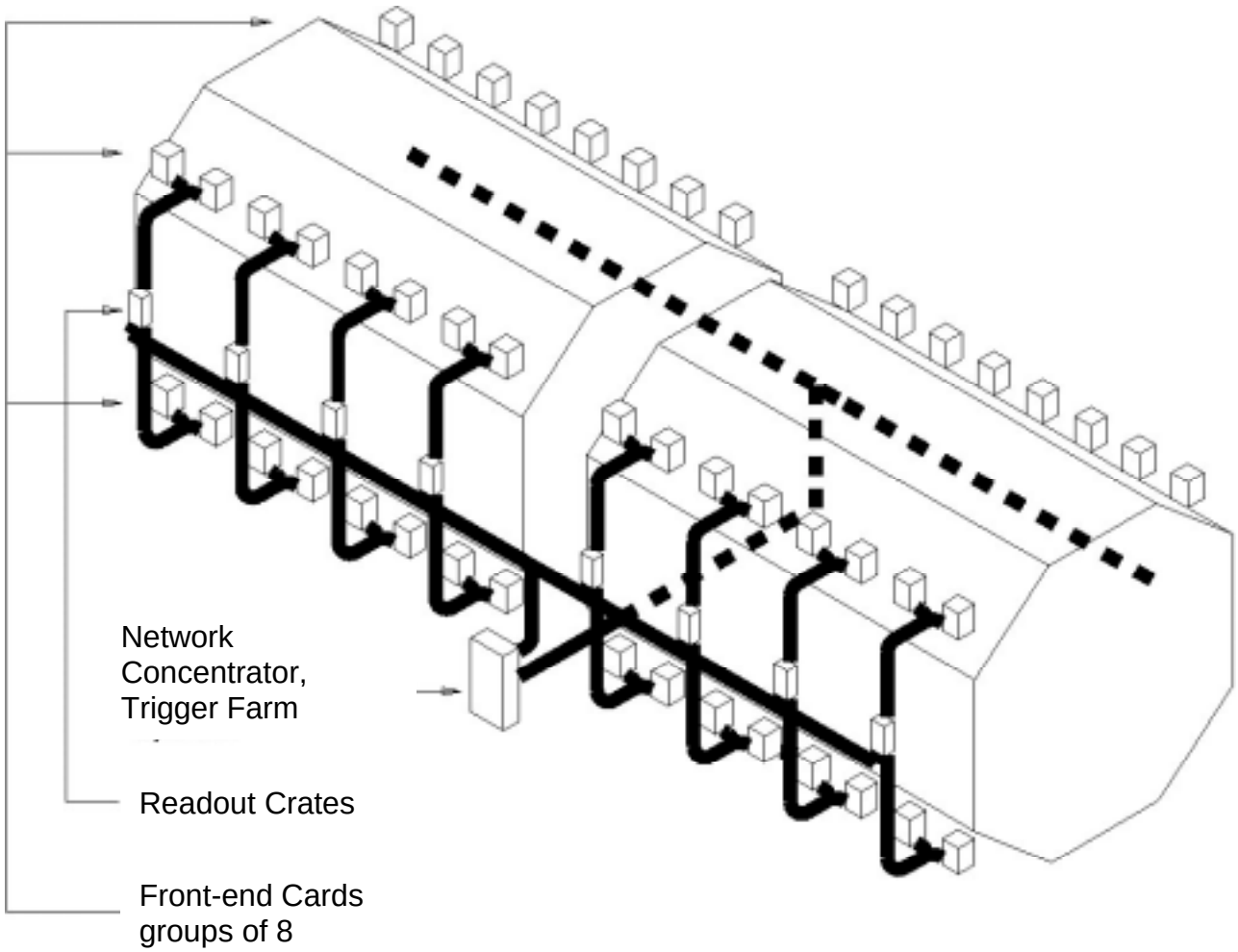


Figure 6.8 Layout of the electronics on the MINOS far detector.

6.4.3 Signal size and dynamic range requirements

6.4.3.1 Anode signals

PMT gain is considerably higher than required for compatibility with VA chip. The PMTs will operate at nominal gain of 1E6 with the low gain pixels operating at no less than 33% of nominal. The maximum signal is taken as 150 photoelectrons which gives us the following:

Qmax = 150 * 10^6 electrons = 24 pC
Qmin = 33% * 10^6 electrons = 53 fC

Thus ratio Qmax/Qmin = 450 (9 bits). Since we require high efficiency at recognizing single photoelectrons, we demand a significantly higher system dynamic range of ~13 bits.

When used with PMTs operating at high gain, we do not expect noise levels in the VA preamplifier (integrator) to dominate since they will be well below 1 fC. VA noise is expected to be dominated by voltage statistics on its sample/hold capacitor. This is given by $\sqrt{kT/C}$ =100 μV.

With the VA's largest signal capability of order ~1V, this gives an effective maximum dynamic range of ~10^4 or 14 bits. IDE estimates maximum dynamic range to be ~13 bits.

6.4.3.2 Dynode signals

If we assume single dynode gain to be 2 - 4, then minimum single photoelectron dynode signal will be ~25 fC. A variety of choices exist for amplifying and discriminating these pulses. An equivalent noise charge level of well under 1 fC is not difficult with shaping times of order 15ns. Various configurations of discriminator can be used for this purpose.

6.4.4 Basic Architecture

6.4.4.1 Front end board

Mounting. Each Front End Board (FEB) is associated with a MUX box and is mounted onto it in a separate shielding enclosure. The front end board mounting is shown in figure 6.9. Front end electronics is thus kept out of the Mux Box, which must be independently light tight.

The idea is to have a printed circuit panel as an integral part of the mux-box. This panel contains connectors facing in to mate with ribbon connectors to the PMT base. It also has connectors facing out which mate with connectors on the front end board using board to board connector hardware (e.g. Samtec "Board Stacker" series)

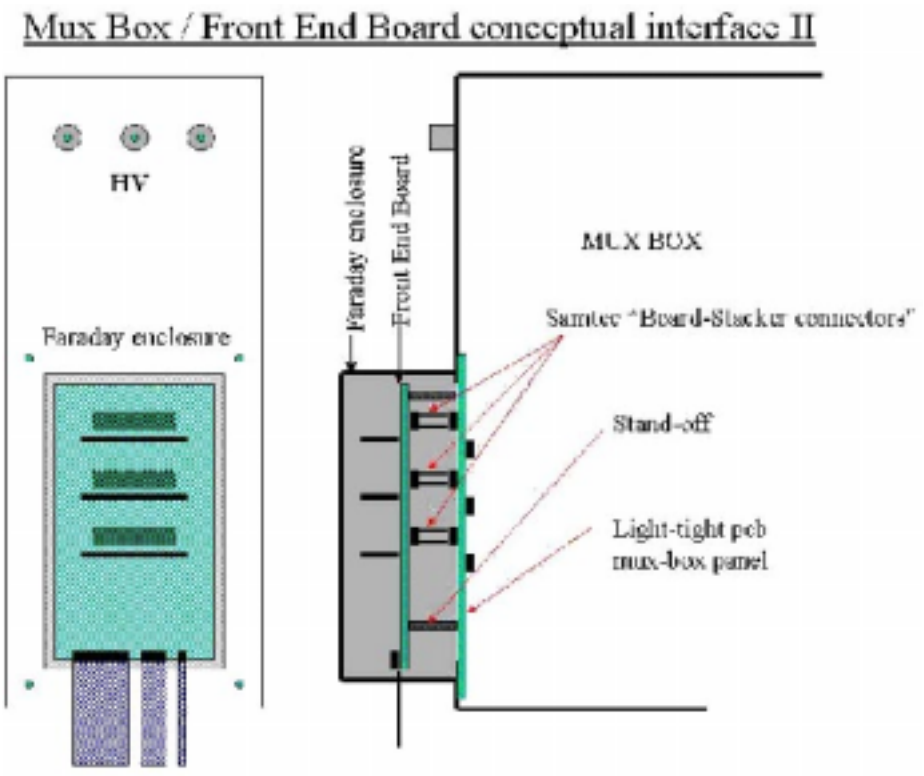


Figure 6.9 Schematic of the mounting of the far front end board containing 3 VA chips to the light tight MUX box.

PIN diode inputs. There will be two pin diodes to monitor for each PMT. Since its signal is expected to be much smaller than the PMT signal, it must be boosted in such a way as to produce a "PMT like" signal. This means that the amplifier output must be high impedance, low capacitance, and have a dynamic range compatible with the VA chip, which will read it out on an unused channel. The calibration light path must also be arranged such that the amplified signal arrives at the VA chip in "reasonable" coincidence with the light in the associated PMT. This is required for proper triggering and we expect that an accuracy of +/- 25 ns will be adequate.

For grounding integrity, it is important that no single ended signals or extraneous ground connection is made to the front end board or its enclosure. Therefore, the PIN diode as well as its amplifier will be mounted directly on the front end board. Light will be brought in by fiber optic.

Dynode trigger. The dynode signal, common to all sixteen channels, will be used to generate trigger signals. At 1E6 PMT gain, the nominal single photoelectron pulse at the anode will be 160 fC. On a low gain pixel, this could be down by 50% to ~80 fC. If we assume the lowest dynode has gain of 2, then the minimum dynode signal will be at least 40 fC. If dynode gain is 4, then this goes up to about 60 fC.

The device which will be used to process the dynode charge is the “ASD-lite”, an amp/shaper/discriminator designed for ATLAS muon system. It is a CMOS chip with a shaper peaking time of 15 ns, a sensitivity of ~12 mV /fC and an Enc of 0.5 fC.

Initial tests with this device show very good results. The device exists in undiced wafer form in large quantity and are available for MINOS.

The readout is based on a general architecture shown below in Fig. 6.10.

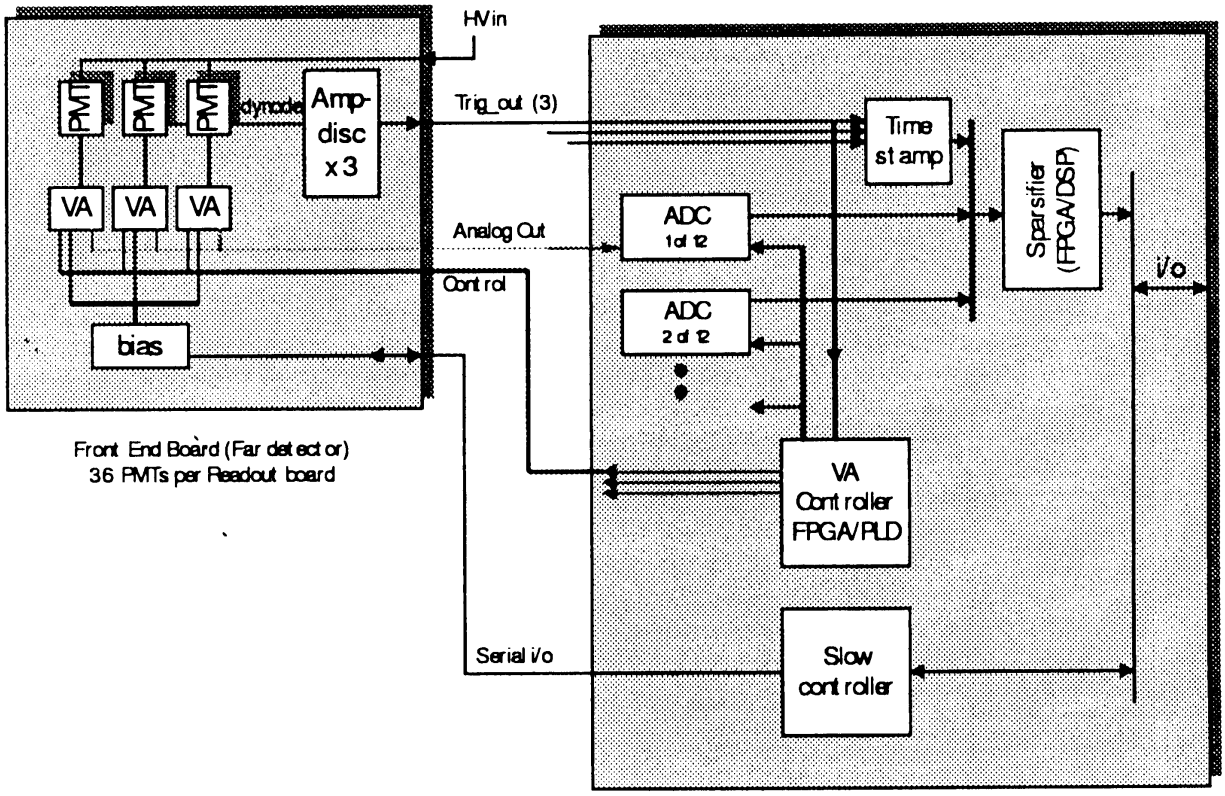


Figure 6.10 Schematic diagram of the components of the far detector electronics system.

6.4.4.2 Readout board

General features. The overall architecture of the readout board is shown in figure 6.11. ADCs are located on Readout Boards, which are located in crates distributed along the detector. Their size and location is dictated by cable length considerations.

The Readout Boards receive the triggers from the FEBs and pass them to a controller FPGA. The controller contains state machines for each ADC channel and is responsible for toggling out the analog data from the VA chip and controlling the ADC. Each trigger results in the readout of all 16 active channels in the VA chip at a rate of 150 ns - 200 ns per channel. The readout time for 16 channels is the total of the shaper peaking time (0.5 - ~1 μs) , readout time of the analog multiplexer ~3 μs, and some recovery time after the readout during which the preamp and shaper levels settle back to pedestal ~2 μs. We thus estimate the total readout time to be ~6 μs.

After VA readout, the ADC data are stored in FIFOs and processed by the Sparsifier (FPGA or DSP). The Sparsifier subtracts pedestals from each channel and passes on nonzero data for VME readout. Pedestal runs will be taken at intervals of approximately one per day and data are stored in on-board memory available to the Sparsifier. This is a typical architecture for VA readout of which numerous examples exist.

Its “front end” is divided into six identical sections each of which has an ADC with 2:1 input multiplexer, a controller with time stamp, and an 18 bit-wide FIFO. Each of these sections services two front end boards. Each ADC is servicing 6 VA chips keeping it busy 3.6% of the time, with no loss of readout rate. We could, in fact, further reduce the number of ADCs, but the cost savings diminish and in the interest of conservatism, we stop at six ADCs per board.

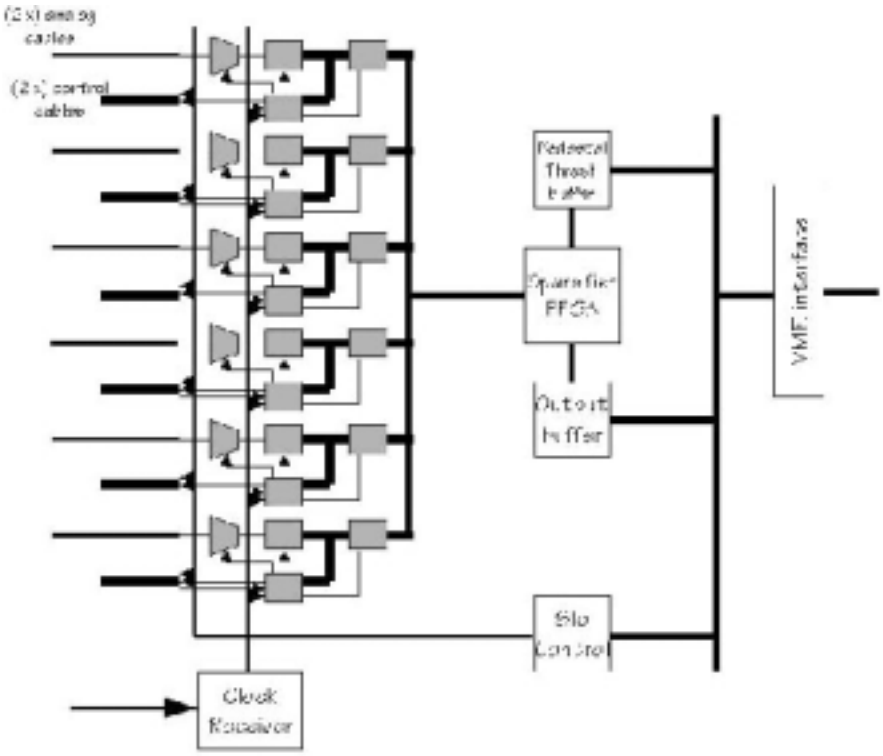


Figure 6.11 Schematic diagram of the far detector front end readout board.

Clock receiver. There are three global timing signals received by the board. All are transmitted to the board via LVDS signals on the backplane of the VME crate. They are generated by the Global Clock Receiver Module in the crate. The received signals are

- 40 MHz CLK : Global timebase
- MARKER : One CLK period in duration, once per second
- CAL : Accurate (~1ns) signal to coordinate timing of cal-injection to front ends.

Time stamp and VA controller. The VA controller will handle following tasks:

- Receipt of dynode triggers from front end boards; six triggers total
- Control of VA chip and coordination of ADC control lines
- Generation of internal 80 MHz clock and 27 bit course counter for time stamp.
- Coarse counter resets on receipt of MARKER signal once per second
- Generation of 4-phase internal clock for time stamp interpolator - 1.5 ns bins.
- Loading of 20 word data packet into FIFO

The VA controller will be implemented in a Xilinx Virtex series FPGA.

Sparsifier. The sparsifier will offload the data FIFOs in round-robin fashion and pack the sparsified data into buffer memory for VME readout. This function will be implemented in a Xilinx Virtex FPGA. The output data will consist of 8 bytes per valid hit. Thus, compared with the 20 word (40 byte) data packets in the FIFOs, the compaction is 5:1. Data blocks will be reported to the DAQ via a status register blocks corresponding to time intervals as opposed to fixed size blocks. Thus, for example, blocks can be downloaded corresponding to 10 ms of data. The time interval will be programmable in 1 ms units.

VME interface. The VME interface will support VME64 block data transfers as well as more mundane operations all the way down to D16/A24. The latter will be useful for preliminary tests using LabView or other commercial operating environment. The interface will be implemented using the Cypress CY7C960/964 “Slave VME Interface Controller” chip set.

6.4.4.3 Cabling

The readout board will have twelve sets of cables going out to the twelve front end boards. Each set consists of:

Digital signals. For reasons of minimizing radiated interference from digital signals, these will be transmitted using the Low Voltage Differential Signal (LVDS). The signals to be transmitted are the VA control signals of which there are about a half dozen, the dynode trigger signals, and the Slow Control signals. Digital cables will be flat ribbon cables on 0.025” pitch.

Analog signals. The VA multiplexer output is a differential current, which must be driven via twisted pair, shielded cable to the Readout Board. There is a potential limitation to the

length of this cable due to cable losses and dispersion. Dispersion manifests itself in a long low level tail in the return to baseline after a large pulse. Measurements of this were done using various lengths of cable of solid dielectric (RG174) and foam dielectric types (RG58A). These cable types are not differential but were used to indicate the effects of dispersion. Return to baseline at the 10^{-4} level, required of a 14 bit system, occurs within a microsecond. The effects are small and can be calibrated out off-line. The cable we propose to use is ~20' expanded PTFE to minimize this effect.

Low voltage power cables. There will be shielded twisted pairs cables to carry the various low voltages needed to the Front end boards.

6.4.4.4 Far detector data readout

Rates in the far detector are dominated by PMT single photoelectrons. We assume a worst case rate of ~1 kHz per phototube. If we assign one ADC channel to each VA chip, as indicated in the basic readout scheme of figure 6.10, the total demand we are placing on the ADC is exceedingly low; the product of PMT trigger rate and VA readout time.

6μs * 1kHz = 0.6%

Given this low demand, its makes far more sense to utilize one ADC channel for two Front End Board containing 3 VAs instead of one per ADC for a total of 6 VA's per ADC chip. This scheme is shown in Fig. 6.10. Since during a VA readout cycle, the remaining VA chips are capable of storing a new incoming signal, there is no additional deadtime incurred in this scheme. A trigger on VA-2, for example, is not lost if the ADC is busy processing VA-1. The sample/hold of VA-2 is activated and the signal remains stored until the ADC is free to process it. Thus, the ADC utilization is 3.6% while the "deadtime" for each PMT remains at 0.6%. This results in a very compact readout with one Readout Board servicing 36 PMTs.

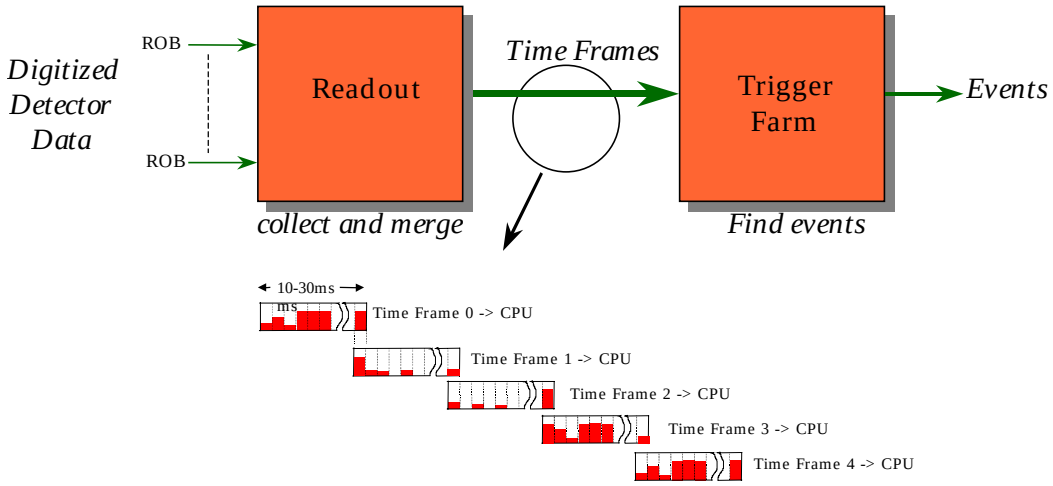
There is some additional complexity in utilizing a single Readout Board for twelve FEBs. One issue is cabling. Each Readout board must receive twelve digital and twelve analog cables. A single width 9U VME board does not have enough panel space for this and so the cabling must be divided between the Readout card and a simple mezzanine card, which is attached to it. The VA controller must also be more complex than in the basic scheme. The controller contains one independent state machine for each front-end board. This state machine keeps track of its three VAs in the manner described. This can be accommodated using high density and high pin count FPGAs or CPLDs.

6.5 Central data system and trigger farm (WBS 2.3.3)

6.5.1 Overview

The principle of the readout system is shown in figure 6.12. The MINOS detectors use a simple, continuously active readout architecture. The amplitude and times of all Photo Multiplier Tube (PMT) signals are digitized by the front end electronics and buffered for readout by the DAQ system. Synchronized time blocks of data from the front end electronics are read out and assembled into longer time frames with small overlaps and passed on to the trigger farm for event selection. Events are transmitted from the trigger farm for storage and analysis.

Figure 6.12 Data flow in backend system. Collects times and amplitudes of PMT signals,



correlates signals in time and space continuously, finds interesting events and passes them to the DAQ for analysis and storage.

While the front end electronics for the Near and Far detectors are substantially different, the DAQ system has been designed to be essentially the same for both and use off the shelf components. The use of software rather than hardware for the triggering allows greater flexibility in event selection and does not require the complexities of hardwired trigger logic or the distribution of fast trigger signals over a physically large distance.

The major components of the electronics system as shown in figures 6.1 and consist of the following:

- Front end Boards
- Read Out Boards
- Read Out Processors
- Trigger Farm
- Timing system

6.5.2 Data rates

The data rate is assumed to be distributed evenly across the detector readout system. Each hit will be represented by 8 bytes of data from the detectors, which includes the timestamp, the channel information, the amplitude and the type of data being transmitted. In the worst case, the readout system is capable of handling 212 Hz of hits per PMT pixel (16 channel PMT) This is more than a factor of three above the expected worst rates which come, predominately, from the tube noise. This results in 5 MHz for 23323 channels in the Far Detector and ~2.5 MHz for the 9408 channels in the Near Detector.

Component	Near Detector	Far Detector	Comments
Worst case Detector rate	2.5 MHz	5 MHz	
Hit Data size	16 bytes	8 bytes	
Detector data	40 Mbytes/s	40 Mbytes/s	
Readout crate rate	2.5 Mbytes/s	2.5 Mbytes/s	1 out of 16 in total
Network data rate	10 Mbytes/s	10 Mbytes/s	1 out of 4 in total
Farm data rates	40 Mbytes/s	40 Mbytes/s	
Farm processor rate	8 Mbytes/s	8 Mbytes/s	1 out of 5 used

Table 6.4 Maximum Rates in the system

6.5.3 Electronics readout system organization

Figures 6.1 and 6.12 show the schematics of the readout system. The system architecture for the Near and Far detectors is essentially the same. Designing the system in this way affords greater simplicity to the system as a whole and greatly reduces overheads in developing, maintaining and running the data acquisition. The design is modular with a strong software component, giving it a high degree of flexibility which copes comfortably with the MINOS requirements.

Up to 16 crates of readout are envisaged in the design for both detectors, though fewer than this are likely to be needed at the ND. The crates have a VME back plane and each contains an on-board processor (the Readout Processor, ROP) that is responsible for the readout, control and monitoring of the Front End Electronics.

Data is taken from the Front End Readout Boards (ROBs) in synchronized Time Blocks of fixed but programmable length and buffered for transmission to the trigger farm over a fast (132 Mbytes/s) PVIC connection (a PCI to PCI transparent bridge). Co-ordination of readout across the processors is performed by the Readout Control (ROC). With the exception of some special running modes (e.g. pedestal or charge injection runs) no data selection or processing is performed in either the ROPs or the ROC. A number of sequential Time Blocks are assembled into larger Time Frames which will contain readout from the entire detector for a fixed but programmable time period. These are passed over the PVIC connection to a farm of PCs (the Trigger Farm) for event selection and data processing. Adjacent Time Frames are overlapped to ensure that no data is lost by splitting the data amongst the farm PCs in this way. A description of the farm and the farm processing is in section 6.6.

6.5.3.1 Readout Processor (ROP)

The Readout Processor (ROP) forms the primary interface between the front-end electronics and the DAQ. Both the near and far detector systems consist of 16 VME crates, each containing one on-board readout processor (ROP). The ROP will be a CES RIO2 8062 VME single board computer based on the Motorola PowerPC 604e processor operating at a minimum of 300MHz (the clock speed will depend on availability at the time of purchase) and running the VxWorks operating system. This board has a single slot, 6U form factor, with an adjacent slot occupied by the PVIC extension module. The RIO2 supports all VME transfers up to A32D32 in programmed I/O and MBLT64 in DMA master mode and provides slot-1 VME controller capability. 10baseT Ethernet is provided for connection to the local area network. The detectors are divided into readout quadrants. Each ROP in a quadrant is connected electrically to the others. The connection from each quadrant to the trigger farm is done using optical links to minimize loses and interference at a longer distance.

As the time stamping in the ROBs is done at fast rates there will be short wrap around periods in the time stamps which have to be related to the real time clock provided by the GPS system. The ROP will add the real time GPS stamps and store the data in its buffer until the trigger farm is ready to accept its data. The synchronized transfer of data from the ROPs to the trigger farm is managed and coordinated by the Readout Control processors

6.5.3.2 Readout Control (ROC)

The Readout Control coordinates the assignment and transfer of data from the readout processors to the farm processors. This could be a single high performance PC connected to all four PVIC chains or could be a single processor on each chain with one acting as the master, depending on the performance characteristics. The transfer of data from the front end needs to be coordinated to ensure that the data from the entire detector

gets passed to a trigger farm processor in a single time frame. The transfer is executed over the four PVIC connections to the front end. The status of the farm processors is monitored so that processor availability may be identified before data transfer is initiated. Data transfer is carried out by the PVIC network cards using Block Memory Addressing and is initiated only by Readout Control.

6.5.3.3 The Trigger Farm

All trigger processing, singles monitoring and real-time calibration processing is performed in the trigger farm. This consists of an array of PCs connected to the readout system by fast PCI Vertical Interconnects (PVIC) . Up to 15 PCs may be connected in this way although it is anticipated that no more than 5 farm processors will be necessary. For a description of the trigger farm and its operation see section 6.6

6.6 Trigger Farm, Event selection and DAQ (WBS 2.3.4)

6.6.1 Trigger Farm

The trigger farm consists of an array of PCs running the Linux operating system connected to the VME Readout Processors via PVIC and to the DAQ PC by Ethernet. The processors in the trigger farm are functionally and operationally identical and perform independently of one another under the Readout Control (input) and the DAQ (output). Each processor maintains information with which it flags its status, an input buffer into which the raw time frame to be processed is transferred, and an output buffer for storing events to be transferred to the DAQ. An event in this context is any self contained collection of data from the farm processing, whether it be a triggered physics event, flasher statistics, monitoring summaries, etc. The format of an event is a header followed by the event data. The header contains descriptive information including the number of bytes in the event and identification of the type of data contained within the event. The output buffer will contain all events extracted from the time frame and is transferred to the DAQ over a network connection when it has filled to a convenient size or, if this occurs first, when processing of the time frame is complete. The format of the buffer is a header containing the buffer length followed by the buffer data.

The task of the trigger farm is to:

- Identify events of interest by filtering the data through trigger algorithms and transmit them for permanent storage.
- Identify calibration data and perform the appropriate processing
- Accumulate and transmit monitoring statistics on the raw data

6.6.2 Farm Processing

When a raw time frame has been transferred into a processor's input buffer, the processor flags its status as busy and processing begins. The data in this time frame represents a complete time slice of readout from the detector but it is not fully time ordered. The first task performed is to complete the time ordering of the data by applying a sorting algorithm. For benchmarking tests a Quicksort algorithm has been adapted to take advantage of the time ordered sub-blocks in the data which has proved to be adequate for the task. However, further work will be done to identify the most efficient sorting algorithm for this task since large gains in processing power can be achieved by any improvement here.

The time ordered data is next scanned to:

- Locate and extract events of physics interest. The flexibility of triggering in software allows all of the MINOS requirements to be met. Any number of trigger algorithms may be written into the processor software, combinations of which can be selected and/or throttled via trigger configuration tailored to the run. Trigger algorithms for identification of physics events are covered in a following section.
- Randomly sample the raw data at a programmable rate for off-line analysis. The sampling is done by copying hits from the time frame and so incurs no loss of data.
- Locate flasher data (from the light injection system) and perform flasher analysis. Hits belonging to a flasher event are easily identified in the time sorted data stream by locating the special PIN diode readout hits which have been flagged in the front end electronics. Each flasher event will be passed to an encapsulated piece of flasher analysis code which will calculate and accumulate the appropriate statistics. This same flasher code will download its output to the event output buffer as a *flasher statistics event* when instructed. The flasher events themselves can also be transmitted for offline monitoring as required, though this will not be standard running procedure.
- Locate and transmit data that the farm is required to take no action on. This allows for the ROPs (for example) to accumulate statistics or perform processing which can be down-loaded in the data-stream.
- Accumulate monitoring statistics on the singles data. Since the farm is the last point in the DAQ at which all the raw data is present, any singles monitoring required must be performed here. Pre-trigger singles rates of raw data hits will be monitored in the farm on a channel basis and periodically written to the event output buffer as a specially flagged event for collection and transmission by the DAQ.

6.6.3 Trigger Algorithm

The trigger algorithm must reduce the data rate by removing noise and other background from the data stream with minimal loss of events of physics interest. The dominant source of background in the data stream is expected to be the singles rate from radioactivity and photo-cathode noise, both of which are relatively easily discriminated from physics events. At the Near Detector the beam spill gate is available in real-time and the front end electronics will tag all in-spill detector hits, so triggering on beam-related events is very easy – all in-spill hits will be accepted as events. The rate of noise hits in the 10μs STE spill is small, so accepting all in-spill hits is entirely practical. Out of spill and at the Far Detector however, a real software trigger is required. Three types of information can be used to achieve this:

- **Time Structure**. Physics events will contain hits that are strongly correlated in time, i.e. the hits will occur within a narrow time gate defined by the propagation time in the scintillator.
- **Spatial Structure**. Physics events will contain spatially clustered and/or contiguously strung hits (showers/tracks) that span a number of detector planes.

- **Pulse height**. Photo-cathode noise will have a lower pulse height (1 p.e.) than hits from a minimum ionizing particle. Imposing a threshold cut on hits allowed to contribute to the trigger is a fast and powerful discriminant against this noise. However, in order to maintain trigger stability, which could be affected by variables such as photo-tube gains and scintillator light yield, no use is made of pulse height in the baseline trigger algorithm used here. A trigger based on summed pulse height could be easily implemented, however, if it were found necessary.

Since the trigger is required to operate in real time, a simple and fast trigger algorithm is required. To illustrate that a practical trigger can be constructed the following 2-stage algorithm was developed:

- a search is made through the readout in time order until a minimum of 3 hits are found to occur within any 50ns window. This window is wide enough to accommodate expected fluctuations in the relative times of hits before the final timing calibration is applied (offline). Simulation studies of neutrino events in the detector have shown that losses to neutrino events from this requirement are less than 0.5%; these losses consist entirely of neutral current events with very few hits. If this condition is satisfied the second, more stringent, level 1 criterion is tested.

- require that at least *M* planes out of any group of *N* contiguous planes of the detector have at least one channel hit in the 250ns following the earliest hit in the above 50ns gate. A 250ns window is chosen here as a conservative event size. If the *M/N* condition is not satisfied the trigger search continues where it left off in level 0. If the condition is satisfied, an event trigger is generated and the event is copied to the event output buffer for collection by the Data Distribution System.

At this stage an event is defined as all hits contained within the 250ns window plus any hits that occurred in a preceding (programmable) time window of T μs. Such a detector history allows the possibility that the event has been corrupted by pileup or that hits have been lost due to single channel dead-time to be assessed. Although this means that the first T μs or last 250ns of each time frame would not be scanned for a trigger (because the pre/post-trigger data will not be present) this generates no trigger inefficiency since the trigger block overlaps ensure that these triggers are found in the preceding or following time frame by another processor.

Studies using the MINOS detector simulation (GMINOS) have shown that this 2-level trigger with M=4 and N=5 excludes a negligible fraction of charged currents neutrino events and around 11% of neutral current events, these being events with very few detector hits. Changes to the (level 1) M out of N plane trigger are trivial to implement in this scheme and will have no significant effect on the algorithm timings. For example if, following further trigger studies, the 4/5 plane trigger used here were required to be a 3/5, 4/6, … plane trigger to accept a higher fraction of neutral current events it could be accommodated easily.

6.6.4 Benchmarking

Prototype trigger processing code for the above trigger algorithm was written in C to estimate the maximum number of trigger processors the trigger farm will require to keep pace with the maximum design requirement for the DAQ. Noise data including an assumed 5kHz double-Compton rate from radioactive decays, were generated at a number of rates up to and including a worst case of 20MHz, well above the DAQ design requirement. The tests were performed with a 3-supermodule MINOS detector (the maximum cavern capacity). Timing tests were performed on a 300MHz ALPHA RISC processor (Alpha Server 1000A 5/300, Alpha 21164 chip) which, even now, is outstripped by considerably faster off the shelf processors. The benchmarking includes time sorting, the trigger search and histogramming of raw channel singles rates for channel monitoring. Calibration processing was not included (e.g. flasher event processing) but this should have only a minor impact.

The results are shown in Table 6.5. The first three columns show the level 0 and level 1 noise trigger rates for a 3/5 plane trigger and 4/5 plane trigger as a function of the detector singles rate. There is no difference in processing requirements for these two different trigger configurations.

The processing requirements are well within practical limits; the provision of sufficient processing power in the trigger farm is not expected to be a problem.

Singles Rate (MHz)	**Trigger Rate (Level 0, kHz)**	**Trigger Rate (Level 1, Hz) 3/5 planes**	**Trigger Rate (Level 1, Hz) 4/5 planes**	**Max Processors**
2	4	6	<1	1
6	70	26	<1	3
10	290	130	<1	5
16	1100	750	<3	8
20	2000	1500	<5	10

Table 6.5 Trigger rates and processor requirements of the trigger farm. The processing power estimates were obtained using an Alpha Server 1000A 5/300, Alpha 21164 chip processor.

6.6.5 Triggered Data

Triggered events are passed to the DAQ from the trigger farm over a network connection using standard TCP/IP protocols. The events can arrive out of chronological order by an amount defined by the maximum length of time it takes a processor to trigger analyze one trigger time frame. In addition, because trigger time frames overlap, some events may trigger twice. The DAQ will buffer the events it receives in a rolling buffer, time

order them and remove or merge (as appropriate) event duplicates and overlaps before passing them on for archival and to online consumers.

The output event rate from beam and cosmic ray muon events will be relatively low. In the far detector the event rate will be dominated by around 1 Hz of cosmic ray muon events (2.4 Kbytes/s uncompressed). The near detector rate is more complex but, for the high energy beam, will average approximately 100 Hz of ν interactions, 10 Hz muons from ν interactions upstream of the target region and up to 270 Hz cosmic ray muons (virtually all out of spill), giving a total rate of just under 400 Hz equivalent to a data rate of about 500 Kbytes/s uncompressed. Cosmic ray muon events are essential for cross calibration of the near and far detectors; the cosmic muon rate at the near detector is quite high and can be reduced by randomly vetoing out-of-spill triggers as part of the near detector trigger algorithm.

6.6.6 Data Acquisition System

The main function of the data acquisition system (DAQ) is to receive events from the detector electronics and record them on a mass storage device. Trigger rates in MINOS are low so the requirements on the MINOS data acquisition system are not demanding. The readout system and trigger farm build events as described above and present them to the DAQ via the Ethernet LAN using conventional TCP/IP protocols. The DAQ resolves any event overlaps caused by the data splitting in the trigger farm before formatting the data into fully structured events and archiving and distributing it to online consumers. The integrity and quality of the data and the performance of the detector are continuously monitored by the online system. An additional PC will be provided at each site to provide the resources required for the online monitoring of the data and detector.

The high level DAQ software (Run Control, Data Distribution and Online Monitoring) will be written using ROOT classes and will run on Linux PC's at both detectors. ROOT is widely used in the community for online as well as for offline systems and offers excellent support for a wide range of classes, including GUIs, I/O, plotting and graphics together with OS support. The graphical user interface provided by ROOT allows an operator interface to be easily built through which data taking runs can be conveniently controlled. The plotting and graphics provide the framework for the online monitoring and the ROOT I/O provides data and file formatting. An additional, major advantage of using ROOT is that it is also the system on which the MINOS offline software will be based. Thus MINOS is provided with a uniform software base and the online and offline can directly share software development tasks. The interactive event display and event reconstruction code developed by the offline group, for example, will be used as part of the online system.

The event data will be transferred directly to the Feynman Computing Center (FCC) from both the Near and Far Detector sites over a network connection where it will be archived and distributed to collaborating institutes as necessary. All bulk offline processing of the data will be performed on the Fermilab computing farms. Local tape drives will be

provided at both detector sites as a backup solution in case network connections to the FCC are temporarily interrupted.

6.7 Database systems (WBS 2.3.5)

The Minos databases will maintain a record of the construction and operation of the detector through the course of the experiment. Some of the information will be recorded only once, or very infrequently; some will be recorded regularly to track detector performance and calibration. Information may be recorded in many ways; some will be entered manually, some will come from automated test equipment, and some will be generated by the various software systems. The data stored in the database must be available to all members of the collaboration, as the database will store the calibration constants needed by the analysis programs.

The architecture of the database is dictated by the experiment; there will be a central server at Fermilab to store all the data, a server at each detector site to supply constants quickly to the trigger farms, and satellite servers at collaborating institutions for analysis. The satellite servers will be owned and operated by the various institutions, with downloads supplied periodically by the Minos database group. The satellite systems will be essentially read-only, although there may be exceptions to this rule. There will also be mini-databases at the factories to store test results locally before uploading them to the central server every night. The mini-databases will allow test equipment to keep running when the Internet connections are down, and let technicians check their data before it goes to the central server.

Information will be entered into the database in many ways. Construction details will be entered manually into web-pages connected to the database either via Java applets or through PHP-Apache http servers. The same system of web-page access to the database will handle the demands of the electronics service technicians, who will use the database to store the repair and calibration histories of every board. While the experiment is running, maintenance technicians will use the web-page system to query and update the database on current construction details. The advantage of the web-based system over a spreadsheet is that we can control access better with a web-based system, and guide users through tables. We can also trap errors and do some validity checking with the web-based system.

There will be a system of objects to access the database through software. Minos software is based on the "Root" system of Rene Brun, et al., so there will be an interface from Root to the database. There will be two levels in this system, a low-level interface called TSQL which will do the actual interfacing and execute SQL strings on the database, and a high-level system called DBI which will answer more abstract queries (it will have a facility to return the complete calibration of the far detector at a given date and time, for example). DBI will also include a facility to supply data from several sources; this will allow overriding the standard calibrations with some special set, for example, as well as letting users specify a series of places to look for data. The Protvino group will supply the code for this system.

Data from the module and phototube test facilities will be entered into the database system through mini-databases at the respective factories. Manual data entry at these facilities will be done through the web page system into the local mini-database, but the larger amounts of data generated by the various test machines must be entered more efficiently. The database entry will either be written into the test machine code (using ODBC calls), or the data will be entered with a bulk-loader program from flat files. In any event, the mini-databases will update the central server nightly. The mini-databases will not contain any other data from the rest of the experiment.

The DCS system will handle database requests and updates from the trigger farms and beamline systems. Communications will be through flat files, which will mean there will always be a set of data on disk, whether the database is operational or not.

Examples of the information that will be stored in the database are given in Table 6.6. The source, level of detail, and a rough guess at the frequency of recording are also given.

Item	Information	Level	Source	Frequency
Construction				
Steel Plates	Chemistry Mass Thickness Magnetics Magnetic field model	Batch Plate Plate Batch Plate	Manufacturer Installation Installation Manufacturer Magnetics group	Once Once Once Once Once
Scintillator extrusions	Construction details Light yield	Batch Batch	Extruder Extruder	Once Once
WLS Fibers	Construction details QC tests	Batch Spool	Manufacturer Module factory	Once Once
Scintillator modules	Construction Dimensions Mapper results	Module Module Module	Module factory Module factory Module factory	Once Once Once
Photodetector	QE, uniformity, gain Operating HV	Pixel Tube	PMT tester PMT tester	Once Once
Electronics	Modification level Repairs Switches Calibration	Board Board Board Board	Factory Repair tech Installation Test rig	As req'd As req'd Once Once
Installation				
Steel Plates	Positions Alignment	Plate Plate	Detector Detector	Once Once
Scintillator modules	Positions Light yield	Module Module	Installation Wire source	Once Once
Photodetector	Gain	Pixel	Light flasher	Once
Electronics	Calibration	Channel	Charge injection	

Item	Information	Level	Source	Frequency
Construction				
Steel Plates	Chemistry Mass Thickness Magnetics Magnetic field model	Batch Plate Plate Batch Plate	Manufacturer Installation Installation Manufacturer Magnetics group	Once Once Once Once Once
Scintillator extrusions	Construction details Light yield	Batch Batch	Extruder Extruder	Once Once
WLS Fibers	Construction details QC tests	Batch Spool	Manufacturer Module factory	Once Once
Scintillator modules	Construction Dimensions Mapper results	Module Module Module	Module factory Module factory Module factory	Once Once Once
Photodetector	QE, uniformity, gain Operating HV	Pixel Tube	PMT tester PMT tester	Once Once
Electronics	Modification level Repairs Switches Calibration	Board Board Board Board	Factory Repair tech Installation Test rig	As req'd As req'd Once Once
Installation				
Steel Plates	Positions Alignment	Plate Plate	Detector Detector	Once Once
Scintillator modules	Positions Light yield	Module Module	Installation Wire source	Once Once
Photodetector	Gain	Pixel	Light flasher	Once
Electronics	Calibration	Channel	Charge injection	
Magnet	coils Induction	Coil	DCS	
Operation				
Scintillator modules	Calibration constants	Along module	Muon fitting	Many times
Photodetector	Gain Replacement history	Pixel Tube	Light flasher Maintenance tech	Daily
Electronics	Calibration constants Disabled channels FPGA and ROM programs Trigger farm software High and low voltages Repair history	Channel Channel Unit PSU Board	Charge injection Maintenance tech Repair tech	
DCS	Alarms Watches Monitors	DCS channel DCS channel DCS channel	DCS DCS DCS	As req'd As req'd As req'd
Magnet	Current Induction coils	Each PSU Plate	DCS DCS	

Item	Information	Level	Source	Frequency
Construction				
Steel Plates	Chemistry Mass Thickness Magnetics Magnetic field model	Batch Plate Plate Batch Plate	Manufacturer Installation Installation Manufacturer Magnetics group	Once Once Once Once Once
Scintillator extrusions	Construction details Light yield	Batch Batch	Extruder Extruder	Once Once
WLS Fibers	Construction details QC tests	Batch Spool	Manufacturer Module factory	Once Once
Scintillator modules	Construction Dimensions Mapper results	Module Module Module	Module factory Module factory Module factory	Once Once Once
Photodetector	QE, uniformity, gain Operating HV	Pixel Tube	PMT tester PMT tester	Once Once
Electronics	Modification level Repairs Switches Calibration	Board Board Board Board	Factory Repair tech Installation Test rig	As req'd As req'd Once Once
Installation				
Steel Plates	Positions Alignment	Plate Plate	Detector Detector	Once Once
Scintillator modules	Positions Light yield	Module Module	Installation Wire source	Once Once
Photodetector	Gain	Pixel	Light flasher	Once
Electronics	Calibration	Channel	Charge injection	
Beams	Magnet currents Protons/pulse	Magnet Pulse	Beamline controls Beamline controls	
Environmental	Temperature Humidity	Detector site Detector site	DCS DCS	

Table 6.6 Examples of the information that will be recorded in the database during the different phases of the experiment.

The size of the database is estimated at around 20 Gigabytes. The bulk of the data will be from calibration constants due to muon fitting and beams monitoring. We expect to use Oracle as much as possible, since Fermilab has a net license we can use. They also have a great deal of experience with Oracle and can help us program the database. The mini-databases at the factories will be either Personal Oracle on NT or MySQL on Linux.

6.8 Detector Control and Monitoring System (WBS 2.3.5)

6.8.1 Scope of the DCS

The MINOS Detector Control System (DCS) will be used to monitor and/or control all slowly varying parameters of all sub-detectors and sub-systems as well as the operational state of the near/far MINOS detector and of the associated experimental infrastructures to maintain the safety of the experimental equipment.

Typical sub-systems include:

- Environmental parameters, such as Temperature, Pressure, etc.,
- Cooling and Ventilation,
- High & Low voltages from commercial and custom made equipment,
- Readout electronics (front and back end),
- Magnet monitoring and control,
- Equipment safety,
- Beam line and accelerator,

The MINOS DCS system it will be flexible, easy to reconfigure or modify, extensible, and scalable. This system will provide a fully automated package to collect, store, present, and distribute monitored data.

The main advantages of a well centralized DCS is the reduction of the manpower requirements for operation of the MINOS experiment, and in particular the far detector.

The MINOS near detector will be located in an underground area whereas the control room will be located in a surface building. For smooth running conditions the DCS will provide a relatively low-cost system of remote monitoring and controlling. The DCS will monitor the experimental conditions locally and then generates alarm signals in the control room when problems are detected, in order to alert users in the control room to take some actions manually or remotely via the provided DCS graphical interfaces.

Monitoring several parameters of the MINOS experiment is critical not only for the offline reconstruction but also for the safe operation of the experiment. This is one of the reasons, the DCS it will run independently of the main Data Acquisition System (DAQ). There will be some connectivity to link information exchange for signals and messages, such as status of the MINOS detector, etc.

The complete DCS system will be built as a number of independent subsystems and will be integrated at the experimental halls (near and far). During the commissioning and operating phases of the experiment the DCS will be partitioned to allow different subsystems to work independently in order to minimize possible interferences. All the subsystems will use the same underlying DCS services (data display and visualization, alarm handler, database, etc.) to create an efficient monitor/control system. Past experience has shown many advantages to designing a DCS system in a highly modular

fashion, with different sub-systems on different processes, and well defined interfaces between them. The modular construction renders the overall DCS system robust against problems in any one subsystem. The modularity will also simplify the interfacing of the DCS system with the external systems, such as the FNAL safety server, Beams Division interface, etc. A modular system it will be influenced by and be significantly helped by the adoption of a commercial industrial Supervisory and Control Data Acquisition System (SCADA), which will be discussed in the next section.

6.8.2 DCS Layout

The MINOS DCS will comprise a physical hardware and a software layer. The physical hardware front-end layer is built from several hardware I/O boards, etc. as shown in the block diagram of Fig. (6.13).

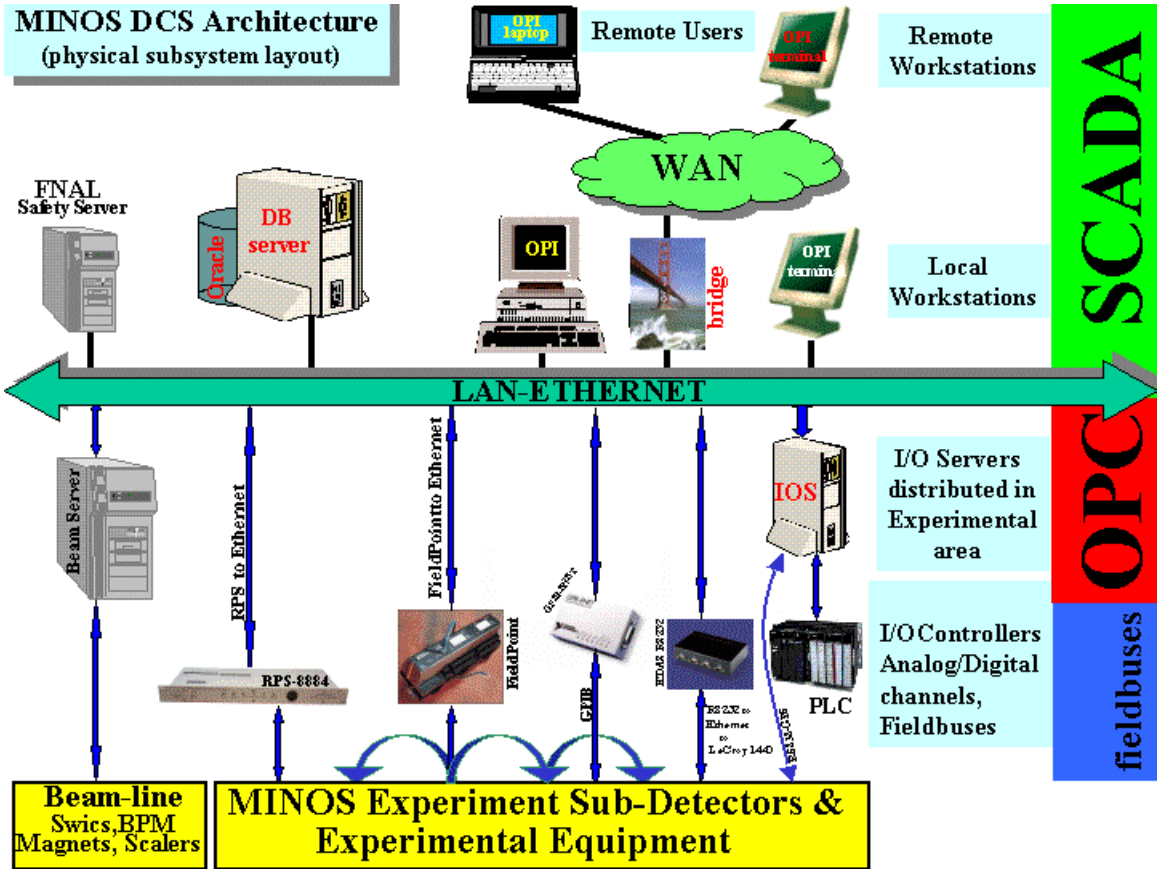


Figure 6.13 MINOS DCS physical subsystem layout.

For the basic MINOS DCS system hardware, a standard configuration of a general control system is followed. The hardware architecture for the MINOS DCS system will be a typical distributed computing architecture. It consists of operator interfaces (OPIs),

Input/Output Controllers (IOCs), and Input/Output Servers (IOSs), tied together by the local area network (LAN-Ethernet) communication link to form a flat network with all nodes as peers. This configuration is presented in the block diagram of Fig. 6.14.

The LAN communication link is the standard Ethernet which ties the IOSs and OPIs together to form a network. The same LAN will be also used by the main DAQ to provide the connectivity with the DCS, Accelerator control/monitor system, FNAL safety server, etc. The IOS will be equipped with a variety of interfaces to various field busses, digital and analog channels, etc. These can be PCs or VME crates. Dedicated process control will be implemented on IOC (Input/Output Controller) Programmable Logic Controllers (PLCs).

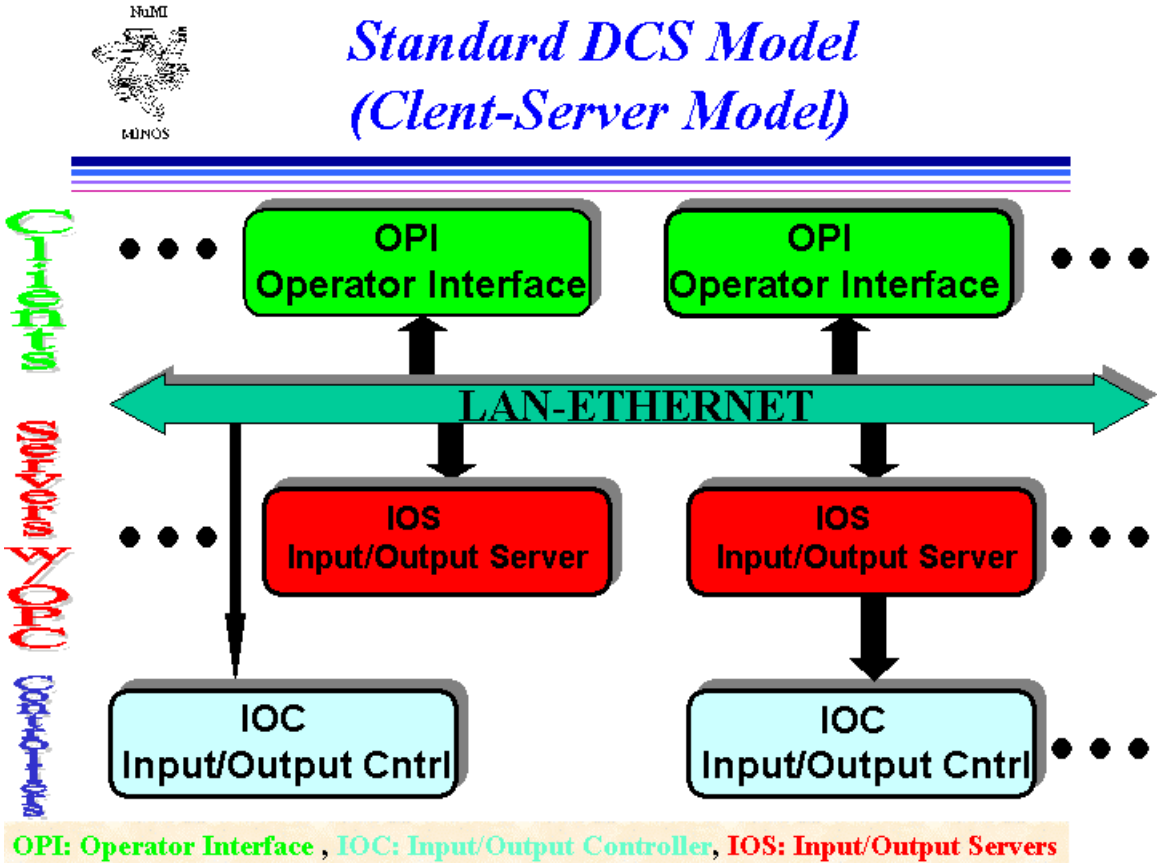


Figure 6.14 A standard DCS software model.

Data from the Accelerator Monitor and Control system will be provided to data servers with the help of the Simple Acquisition of Data services (SAD) from the FNAL Beams Division.

The IOS and OPI will run on color graphics PC, which will be running Windows NT operating system.

The IOS will be distributed around the experimental area, running OPC (OLE [Object Linking and Embedding] Process Control) [15] servers. OPC is an open interface standard defined by the OPC nonprofit foundation. There are already 120 members embracing this foundation including CERN and Microsoft (which is the guarantor of conformity of the standard with the Windows operating system). The aim of OPC development is to build on the Windows-based technology of OLE (Object Linking and Embedding), COM (Component Object Model) and DCOM (Distributed Component Object Model) and to create an open interface that enables simple and standardized exchange of data between the OPIs and the front ends devices. The intention is to make OPC the link between the application programs of the industrial and office sector on the one hand and the world of automation (automation systems, field devices, etc.) on the other.

A commercial, industrial automation, SCADA system running on the OPIs will be used. The iFIX product from Intellution [16] has been chosen. With easy configuration and full OPC connectivity, iFIX SCADA provides an easy way to build experiment control systems. By using the iFIX SCADA, we will to reduce engineering as well as lower maintenance and support effort.

The iFIX SCADA system, as any other SCADA system, consists of two main processes. An event-driven engine maintains the real-time database, communicates with device OPC servers, logs historical data, and processes alarm information. The user process displays the operator interface and executes processes, (written in C, C++, or Visual Basic), that are defined for advanced control algorithms, supervisory control, analysis, and visual presentation.

The main DCS subcomponents are explained in the following subsections.

6.8.2.1 Front End Electronics

Ethernet to VME communication will be provided for the front-end electronics system to be used for the monitoring and controlling.

6.8.2.2 Magnetics

The magnetic field of the MINOS detector will be read out via standard Hall probes in various places along the detector. Digital Tesla Meters (DTM) will digitize the Hall probe information and the GPIB interface of the DTM will provide a way to obtain the magnet information into the SCADA system. The GPIB-ENET (Ethernet GPIB Controller for PCs and Workstations) controller from National Instruments will be used to convert the SCADA system into a GPIB Talker/Listener/Controller (TCL). National Instruments also provides an OPC server for the GPIB-ENET controller.

6.8.2.3 High Voltage

The High Voltage for the PMTs will be provided by the LeCroy 1440 HV system. This configuration requires no special interface to connect the power supply to the PC. A local Ethernet to serial converter will be used to attach each LeCroy 1440 box system to Ethernet.

The 1440 system is a multichannel, programmable high voltage system that provides up to 256 channels of high voltage in each main frame. Up to 16 mainframes may be controlled and monitored via a single daisy chained RS232 connection, although MINOS will need at most 6. The 1440 system operates with the model 1445 controller. This controller provides serial and parallel connection interfaces.

In order to use the LeCroy 1440 with the iFIX SCADA system, an OPC server to communicate over an RS232 serial line was developed by the Alice LHC experiment. The software architecture of the LeCroy OPC server is described extensively in reference [17].

6.8.2.4 Relay Racks

The monitoring of the various Relay Racks along the near and far detector will be done by using the BiRa model 8884 Rack Protection System (RPS) [18]. This model is a detection system designed for the measurement, announcement and control from potentially damaging conditions inside an equipment Relay Rack (RR). The Model 8884 protects the Electronics equipment from excessive heat, water/humidity damage, and smoke/fire damage, etc. The RPS provides a warning and a alarm status. Any combination of individual warnings or alarms can be selectively enabled or disabled.

The RPS is capable of monitoring 12 DC voltages and 3 AC voltages in a rack. The voltage can range from 2V to 24V DC with a resistor value in main chassis being changed for the various voltages being monitored. This model 8884 was originally designed and used by the D0 experiment, and BiRa systems has improved it for a wider usage.

The implementation of the RPS is such that detection of a fault condition first sends a warning alerts and instigates automatic shutdown only if the fault increases in severity to an alarm state. This “two-step” approach allows for manual intervention before automated response, which can reduce false shutdowns. There are two main components in the RPS: the Main Chassis and the Relay Box. The RPS initiates a sequence of steps resulting in a power shutdown when an alarm occurs by disconnecting the AC power from all loads in the protected rack except the RPS.

6.8.2.5 Database

The iFIX SCADA system maintains its own real time database. Some of the DCS subsystem data will be recorded in the MINOS online Oracle database so it can be accessed during the offline analysis as well as during the data taking period, in order to

correlate physics data with some DCS variables, currents/voltages, environmental parameters, etc.

The communication between the SCADA system and the online Oracle database can be done using Structured Query Language (SQL), after installing Oracle client software for Windows NT.

6.9 Far Detector Clock and Distribution System (WBS 2.3.6)

6.9.1 System Description

The clock distribution system is required to provide synchronized timing, referenced to GPS time, across the far detector. A 40MHz clock is needed at the 16 front-end 9U VME crates. Figure 6.15 shows a system diagram.

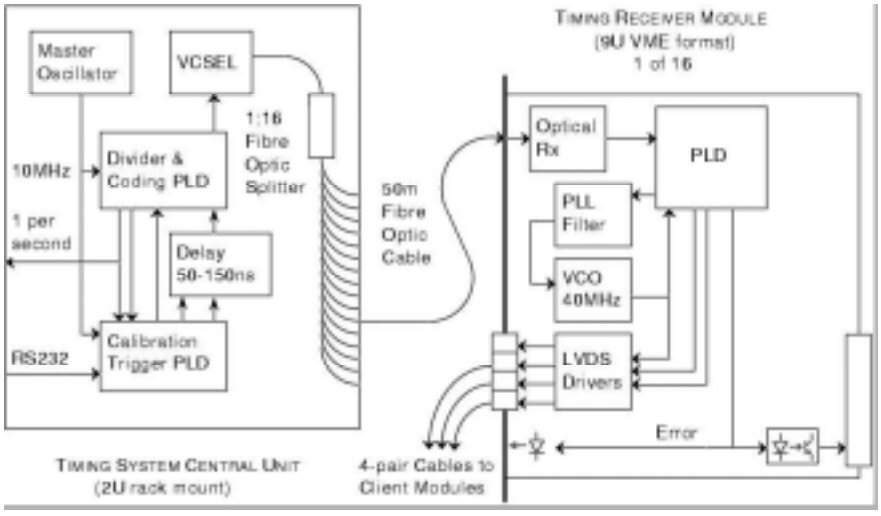


Figure 6.15 System diagram of the GPS timing and clock distribution system for the Far Detector.

Distribution is optical over 62.5/125 μm fiber, from a central unit to VME-format receiver modules in the destination crates. Output from a Vertical Cavity Surface Emitting Laser (VCSEL) is split by an optical coupler onto separate 50m long fiber cables, one to each crate.

Timing is distributed as a single 10MHz pulse-width-modulated signal from which a 40MHz clock, a once per second tick, and an arbitrarily timed calibration trigger are recovered. The encoding scheme ensures reliable operation, and avoids interference between the different functions: it will not be further discussed.

The tick allows time to be obtained by counting clock cycles: it gives the fine part of the time, the coarse part being distributed over the computer network by NTP. The

calibration trigger can be used to caused charge injection, and so give an efficient check of the functioning of timestamping, with reasonable (~10ns) system-wide accuracy.

The timing is derived from a GPS receiver which can also timestamping capability.

6.9.2 Central Unit

The source of the timing signal is a central unit. This receives the GPS clock, from which it generates the composite timing signal. The signal is fed to a VCSEL, giving sufficient power that it can routed by a passive optical splitter in the central unit to separate front panel connectors for each of the 16 destinations.

The 10MHz output from the GPS clock is used to give the 10MHz carrier frequency, and the 1 per second tick. These are combined, along with a calibration trigger input, to give the output signal, and fed to the VCSEL for distribution (Honeywell HFE4080- 322/XBA). The tick is also put on another optical output, to go to the GPS receiver where it will be timestamped. These functions are implemented in a PLD (Xilinx XC95108).

The calibration trigger is formed in another PLD (also an XC95108). This is controlled through a serial interface from an RS232 port. It uses the clock signals to generate a trigger at the requested time, with a 100ns resolution. It also controls a programmable delay chip (type AD9501), which adds additional delay, adjustable with 0.5ns resolution.

The unit is built in a rack mount case, 2U high. The small printed circuit board, power supply, and master oscillator are fixed on the bottom plate. The optical splitter is also mounted on the bottom, with its input fiber looped round to the VCSEL mounted in the middle of the printed circuit board, and the output fibers looped to 16 couplers mounted on the front panel.

Some minor ancillary functions are also included. In particular, it provides the RS232 to fiber optic interface needed to control the GPS receiver on the surface.

6.9.3 Receiver Module

The receiver module is a 9U VME card.

The timing signal comes in on a multimode fiber through an ST connector to an analog optical receiver (HP HFBR-2416) mounted through the front panel. The output goes through a fast comparator to a Xilinx PLD (XC95108).

A PLL locks to the ‘on’ transition of the optical input, and multiplies the frequency from 10MHz to give the required 40MHz output. The phase and frequency detector and

the divider are in the PLD, with an output through a loop filter to control a packaged VCO (e.g. from Mini-Circuits).

Logic in the PLD decodes the modulation, to extract the 1 second tick and the calibration trigger from the composite timing signal.

The outputs are converted to LVDS levels for local distribution. Front panel connection is preferred, with a separate shielded RJ45 connector for each destination module. Connection with a harness on the rear of the VME backplane, employing the 'user defined' J2 pins is possible as an alternative.

A front panel LED shows the PLL is locked, and hence that the distribution system is working correctly. This signal is also available on an isolated open collector output so it can be monitored.

The module will take a local crystal oscillator, so it can be put into a special test mode allowing operation of the supported crate independent of the timing distribution system.

6.9.4 GPS System

The primary time reference for both detectors is provided by GPS timing receivers. This allows events to be correlated with the accelerator spill during off-line processing. For single turn extraction, at least ~1 μs accuracy is desirable in case beam properties vary during extraction, making GPS the obvious method. It is both easy and cheap. The typical accuracy of 100ns is more than adequate, though not sufficient to associate an event with a particular RF bucket. This is attainable, but the marginal benefit does not justify the extra cost.

The GPS timing receivers will be of the type that can record the GPS time at which an external input signal is applied and has a 10MHz output. Typical examples are the HP HP59551A and the TRUETIME XL-DC with event timing option. An RS232 serial connection allows these timestamps to be read out, as well as providing control functions: it will be connected to a PC.

The receiver is used to record the GPS time of the signal used as the reference for timing in the detector. On the far detector this is the once per second pulse; on the near detector this or the spill signal might be used. The time of the spill signal will in any case be recorded.

The PC maintains an internal clock synchronized with GPS. This is propagated over the computer network, using NTP or a similar (possibly simpler) protocol. All processors, including those in the front-end crates, will be able to steer their clocks with an accuracy of ~10ms. The PC also keeps track of the relationship between the local

timing reference and GPS. This allows the relatively short period hardware timestamps to be unambiguously converted to the corresponding GPS time.

The GPS receivers will be underground, with the antennae on the surface. They will be connected over fiber-optic link which carries the optically encoded antenna output. This is converted back to an electrical signal at the receiver. A single fiber is required, plus spares; a single mode fiber will be needed.

6.10 Near Detector Clock and Distribution System (WBS 2.3.6)

6.10.1 Functionality

This system has not yet been designed in detail; only draft specifications currently exist. Figure 6.16 shows the layout.

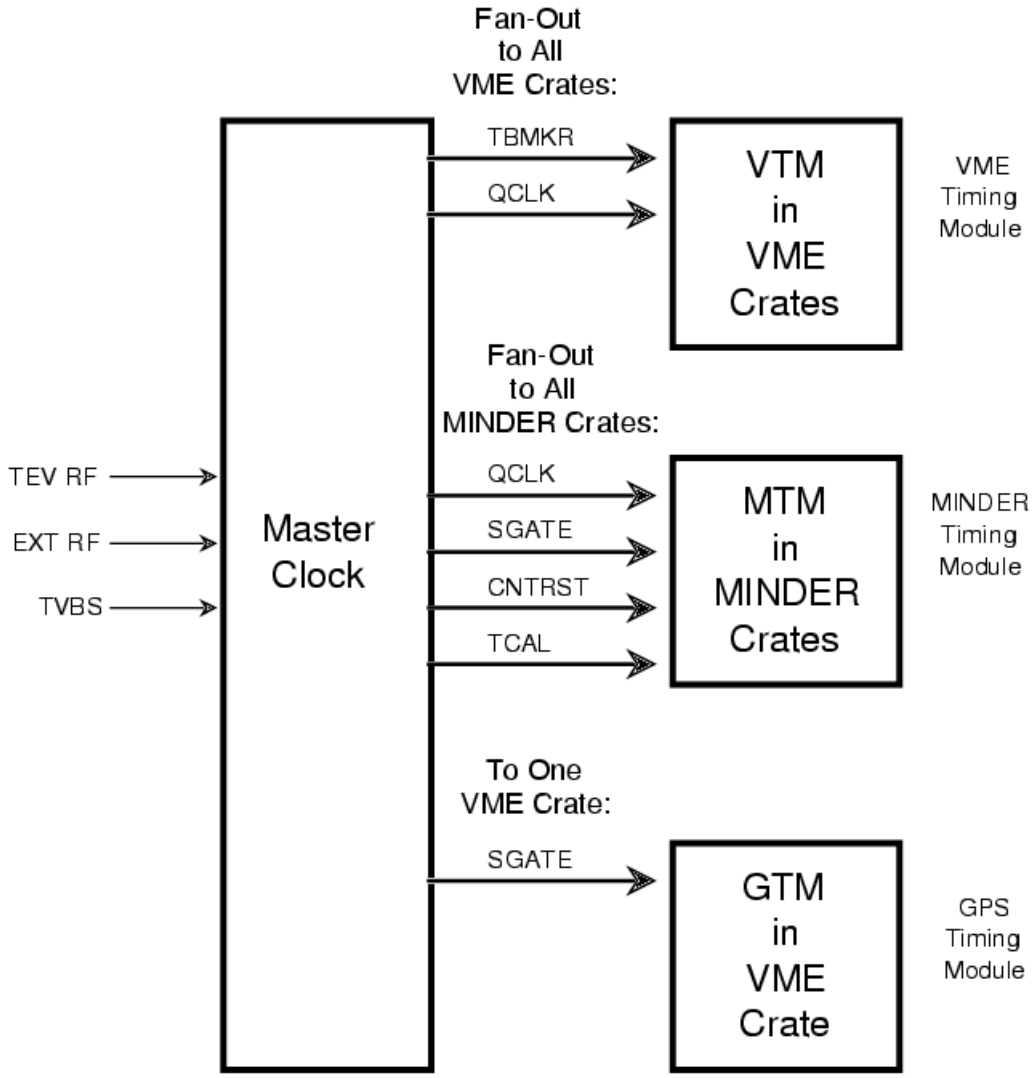


Figure 6.16 System diagram of the Near Detector clock distribution system.

The Master Clock will receive the 53MHz RF from the Main Injector as well as its spill gate. This information will be fanned out to receiver cards in each of the Readout

crates and in each of the Front-end crates. The spill gate will also go to the GPS system to be timestamped. All signals will be transmitted electrically as LVDS. The Master Clock will have an internal oscillator which will allow operation independently of the accelerator (e.g. debugging).

The Front-end cards use the 53MHz signal to clock the QIE chips to provide one digitization every RF bucket. They also receive the spill gate to be able to set there readout mode. Synchronized Reset and Timing Calibration signals are also provided.

The Readout crate receives the 53MHz clock from which it derives the clock used in the data transfer from the Front-end cards. The Time Bank Marker signal is used at the Readout crates to time the switching of the readout data buffers.

Programmable delays will be provided on most of the signals to insure that the timing pulses arrive synchronously across the whole detector (or so that they arrive sequenced at the speed of light as the beam particles do.) Provision are included so that time bank markers, counter resets and timing calibration signals don't arrive during a spill.

6.10.2 GPS System

The GPS system for the Near detector will be similar to the Far detector's. It will however not provide the Master clock signals since these must come from the Main Injector Accelerator. It will provide timestamping of the accelerator spill signals for offline timing synchronization.

6.11 High Voltage System (WBS 2.3.7)

The High Voltage for the PMTs will be provided by the LeCroy 1440 HV system. The 1440 system is a multichannel, programmable high voltage system designed for large-scale applications where high reliability and performance are vital, as in MINOS experiment. The system provides up to 256 channels of high voltage in each main frame (crate). Up to 16 mainframes may be controlled and monitored via a single daisy chain RS232 connection. Control may also be exercised from CAMAC or a PC computer via a parallel I/O port. The 1440 system operates with the model 1445 controller. This controller provides serial and parallel connection interfaces. The high voltage is provided by the model 1443 modules, which have 16 independently controlled high voltage outputs. Each output can go up to 2.5kV and put out up to 2.5mA. We will be using <1000V and <1mA per channel.

We will use a single channel of HV for each phototube - M-16 at the Far and M-64's at the near (3/channels per Far MUX box). This insures that tubes can have their gains independently adjusted both initially during installation process and also as the experiment progresses and the tubes age, possibly at different rates.

For the far detector there will be 8 1440 mainframes which will be situated on the 'half height' walkways along the detector spread along the 2 supermodules. Each will contain 12-16 HV cards. For the Near detector we will use one 1440 mainframes. They will be placed them on the same walkway as the mux boxes, but at the end of the detector, where there is more available rack space. Each of the near detector mainframes will contain 13-16 channel HV cards.

The 1440 mainframes' outputs will be connected to the MUX boxes with RG-58 cable with SHV connectors.

Our application is similar to that of the MACRO experiment which has had extensive experience with a system of ~1000 channels of this 1440 hardware for over a decade. They have seen a failure rate of 16 channel modules at the fraction of a percent (~0.2%) per year level. We have MACRO collaborators on MINOS and will make use of their experiences. One such lesson is that it is essential to have clean AC power provided to the high voltage system. We plan to use Sola-style saturated core ferroresonant transformers as power conditioners. These passive devices will not only be able to remove spikes on the line, but also compensate for variations in the AC voltage.

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[14] Information about the DART system can be found at the URL http://www-dart.fnal.gov:8000.

[15] “OPC foundation”, extensive information can be found in the OPC web page,

http://www.opcfoundation.org

[16] More information can be found in the Intellution web page, http://www.intellution.com

[17] Communication with Benoit Perrin (CERN). Also, view document at http://consult.cern.ch/alice/Internal Notes/1999/42/abstract or view “Documents” in http://klong2.physics.wisc.edu/theoalex/dcs_web

[18] “Rack Protection System - 8884” from BiRa Systems, 2404 Comanche NE, Albuquerque, NM 87107, tel: (505)881-8887, fax: (505)888-0651